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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,801	02/18/2004	Makoto Ogawa	12377/6	9632

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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,801	OGAWA ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11-22 are pending. Claims 1-10 cancelled as per Applicants request.

Specification

2. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. In Claim 19, Line 4, "the instruction codes" lacks antecedent basis in the claim, and is believed to correctly read "instruction codes", and has been assumed to read as such for the remainder of the Office Action. Appropriate correction is required.

5. In Claim 19, Line 11, "the optional instruction" lacks antecedent basis in the claim, and is believed to correctly read "an optional instruction", as has been assumed to read as such for the remainder of the Office action. Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 11-18 is rejected under 35 U.S.C. 102(b) as being anticipated by Rotenberg et al. (herein Rotenberg).

7. As per Claim 11, Rotenberg teaches: An information processing unit,

adding instruction codes which are different from each other in the same group of instruction to each instruction, and sorting the instructions executable into a plurality of groups of instructions (Section 2.2, instruction traces), with the instruction codes which are different from each other in the same group of instruction being added to each instruction (Section 2.2, the Line Fill buffer, which takes instructions and adds them to a trace (group) with a tag. It is unclear based on the applicants specification and claims what an instruction code is, it appears to be a tag, and is assumed as such for the remainder of this Office action),

comprising a decoder circuit selecting the group of instruction corresponding to the instruction code inputted thereto (Section 1.1), based on input history of the instruction code, to determine the instruction to be executed uniquely by the instruction code inputted thereto (Section 1.1, if a trace is encountered more than once, it is executed), and

setting a prescribed instruction code, which assigns an optional instruction depending on the other group of instruction, to each group of instructions (Section 2.2, the trace fall-through address and the trace target address), and wherein said decoder circuit controls to execute the instruction which is assigned to said prescribed instruction code, when said prescribed instruction code is inputted (Figure 1).

8. As per Claim 12, Rotenberg teaches: The information processing unit according to claim 11, wherein said instruction depending on the other group of instruction, which is assigned to said prescribed instruction code, can be changed (Sections 2.1 and 2.3).

9. As per Claim 13, Rotenberg teaches: The information processing unit according to claim 11, wherein a plurality of said prescribed instruction codes, which assign optional instructions depending on the other group of instruction, are provided to groups of the instruction (Section 2.2).

10. As per Claim 14, Rotenberg teaches: An information processing unit,

adding instruction codes which are different from each other in the same group of instruction to each instruction, and sorting the instructions executable into a plurality of groups of instructions (Section 2.2, instruction traces), and

comprising a decoder circuit holding a prescribed information corresponding to input history of the instruction codes (Section 1.1), selecting the group of the instruction corresponding to the instruction code inputted thereto, based on said prescribed information, to determine the instruction to be executed uniquely by the instruction code inputted thereto (Section 1.1, if a trace is encountered more than once, it is executed),

wherein said decoder circuit changes said prescribed information temporary, when a prescribed instruction code is inputted (Sections 2.1 and 2.3).

11. As per Claim 15, Rotenberg teaches: The information processing unit according to claim 14, wherein said decoder circuit determines the instruction to be executed, regardless of said prescribed information corresponding to the input history of the instruction codes, when an instruction code for determining the instruction to be executed uniquely by only the instruction code inputted thereto is inputted (Section 2.2).

12. As per Claim 16, Rotenberg teaches: An information processing unit executing an instruction which is determined by an instruction code inputted thereto,

comprising a decoder circuit holding a prescribed information corresponding to input history of a plurality of instruction codes inputted thereto (Section 1.1), determining the instruction to be executed uniquely, based on the instruction code inputted thereto as well as the prescribed information, from a plurality of instructions which are assigned to the said instruction code inputted thereto (Section 1.1, if a trace is encountered more than once, it is executed, otherwise, another instruction is).

13. As per Claim 17, Rotenberg teaches: The information processing unit according to claim 16, wherein the instructions executable are sorted into a plurality of groups of instructions (Section 2.2, instruction traces) and the instruction codes which are different from each other in the same group are added to each instruction (Section 2.2, the Line Fill buffer, which takes instructions and adds them to a trace (group) with a tag).

14. As per Claim 18, Rotenberg teaches: The information processing unit according to claim 16, wherein said decoder circuit determines the instruction to be executed, regardless of said prescribed information corresponding to the input history of the instruction codes, when an instruction code for determining the instruction to be executed uniquely by only the instruction code inputted thereto is inputted (Section 2.2).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg, in view of Patterson et al. (herein Patterson).

17. As per Claim 19, Rotenberg teaches: An information processing unit,

wherein the instructions executable by said processor are sorted into a plurality of groups of instructions indicated by a group code (Section 2.2, instruction traces), with the instruction codes which are different from each other in the same group of instruction being added to each instruction (Section 2.2, the Line Fill buffer, which takes instructions and adds them to a trace (group) with a tag), and

wherein said each processor comprises a decoder circuit (Section 1.1) which determines the instruction to be executed uniquely based on said group code corresponding to input history of the instruction codes and the instruction code inputted thereto (Section 1.1, if a trace is encountered more than once, it is executed), and

a processor element which executes an operation corresponding to a control signal supplied from said decoder circuit (Figure 1), and

wherein the instruction executable by said processor includes an alias instruction which assigns in advance the optional instruction for the internal instruction code generated by the group code and the input instruction code (Section 2.2, the trace fall-through address and the trace target address), but fails to explicitly teach:

comprising a plurality of processors which execute instructions independently in one chip.

Rotenberg teaches a superscalar machine which can execute multiple instructions in one clock cycle, but does not teach having multiple processors in this system. However, Patterson teaches that the practice of using multiple processors is having a bigger role, due to being able to increase performance at a minimum of cost, and that the complexity of making processors more superscalar becomes a barrier (Pages 635-636). Given the advantage of increased performance for reduced cost, it would have been obvious to one of ordinary skill in the art to apply Rotenberg's invention to a machine with multiple processors, to further increase parallelism.

18. As per Claim 20, Rotenberg teaches: The information processing unit according to claim 19, wherein said each processor further comprises a group resister which stores the group codes set on the basis of the input history of said instruction code (Resisters are inherent in circuits).

19. As per Claim 21, Rotenberg teaches: The information processing unit according to claim 20, wherein said each processor further comprises a look up table which defines the rule for changing the group code stored in said group register (Section 2.2 and Figure 4).

20. As per Claim 22, Rotenberg teaches: The information processing unit according to claim 21, wherein said look up table defines a combination of an instruction mask for setting bit to be masked, an instruction code for comparing the instruction with the internal instruction code generated by the group code and the input instruction code, and a changed group code (Section 2.2 and Figure 4).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must

also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

22. Kahle (USPN 6,697,939) teaches a processor which groups instructions together, and after execution, modifies the groups according to a history.

23. Wirthlin et al. teaches a reconfigurable computer with a reconfigurable instruction set which can be modified and grouped together.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
Art Unit 2183

RF

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